

RIDWAN CHENDARMA C.

ADDRESS NOT FOR PUBLIC VIEW, 626-823-8880, RIDWAN@CHENDARMA.COM

OBJECTIVE

An entry level engineering position related to signal processing, hardware and software implementations, computer programming.

EXPERIENCE

1/5/2009 TO CURRENT California State Polytechnic University, Pomona *Pomona, CA*

MASTER THESIS STUDENT RESEARCH

- Title: FPGA Implementation of Digital OFDM Modulator and Demodulator System
- Build high-performance, high-speed, low-power ADC and DAC system
- System level design using MATLAB Simulink and Xilinx System Generator

1/5/2009 TO CURRENT California State Polytechnic University, Pomona *Pomona, CA*

PROJECT RESEARCH ASSISTANT

- Title: Smart Antenna Angle of Arrival Estimation (Presented to The Raytheon Company)
- Simulate antenna Angle of Arrival estimation using MATLAB
- Methods: Bartlett and Capon Beam-forming. Linear Prediction or Autoregressive Method. MUSIC Algorithm and ESPRIT Algorithm (In progress)

9/27/2004 TO 9/26/2005 California State Polytechnic University, Pomona *Pomona, CA*

UNDERGRADUATE SENIOR PROJECT

- Title: NASA Pair Grant Autonomous Robotic Rover for Planetary Exploration
- Member of Firmware Team. Developed and implemented a controller unit for the rover. FPGA was used as controller unit and coding was done using VERILOG Hardware Descriptive Language.
- Implemented a UART (Universal Asynchronous Receiver and Transmitter) VERILOG code for serial communications between main CPU and FPGA.
- Implemented a state machine in VERILOG code to process input commands and outputs signals to H-Bridge for wheel rotation and to servo-motors for wheels and pan-tilt camera positioning.

EDUCATION

3/5/2007 TO 3/2/2009 California State Polytechnic University, Pomona *Pomona, CA*

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING COMMUNICATIONS AND SIGNAL PROCESSING OPTIONS

MAJOR GPA: 4.00 / 4.00 COURSEWORK COMPLETED, PROJECT/THESIS IN PROGRESS

3/3/2003 TO 3/6/2006 California State Polytechnic University, Pomona *Pomona, CA*

BACHELOR OF SCIENCE IN ELECTRICAL ENGINEERING COMPUTER SYSTEMS OPTIONS

MAJOR GPA: 3.70 / 4.00 OVERALL GPA: 3.27 / 4.00

President's Honor List for 2003-2004 & 2004-2005 academic years, Dean's Honor List every quarter.

MAJOR COURSEWORK

Graduate Level Courses: Microwave Solid State Circuit Design, Numerical Modeling, Stochastic Processes, Advanced Communication Systems, Robust Control, Wavelet Theory and Applications, Systems Theory, Digital Signal Processing, Digital Image Processing. DSP Application LAB, PIC Microcontroller LAB.

Undergraduate Level Courses: Digital Design using VHDL, Computer Organization, Computer Architecture, Application Development using JAVA, Communication Systems, Advanced Control Systems

SKILLS

Programming/CAD: MATLAB/SIMULINK v7.1 & v2006a, XILINX ISE v7.1 & v8.1 with ModelSIM v6.0 (VERILOG HDL), XILINX System Generator v8.1, PIC Microcontroller C Compiler, Microsoft Visual Studio 2005 (C++), Eclipse SDK v3.3 (JAVA), OrCAD Capture CIS v15.7

Laboratory Equipment: Oscilloscope, Function Generator, Multi Meters.

OS Platform: Windows XP, Unix/Linux CentOS with gcc version 4.1.2

References and recommendation letters are available on request.